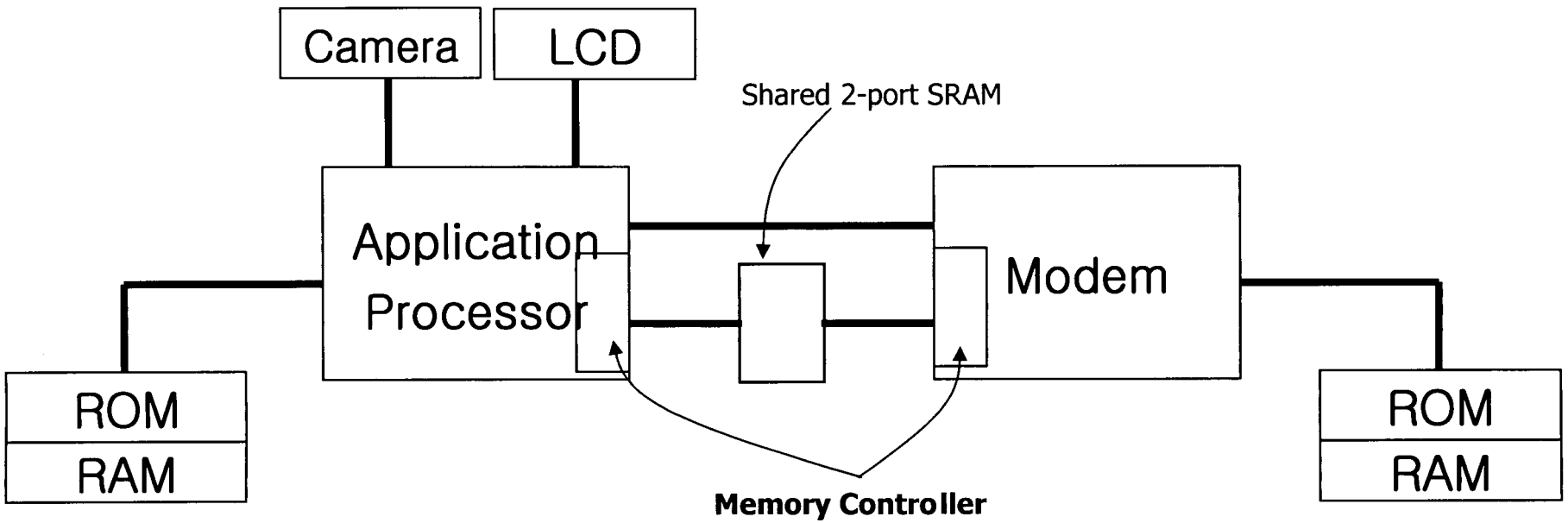
Camera
LCD
Shared 2-port SRAM
Application Processor
Modem
ROM
RAM
ROM
RAM
Memory Controller

Fig. 1

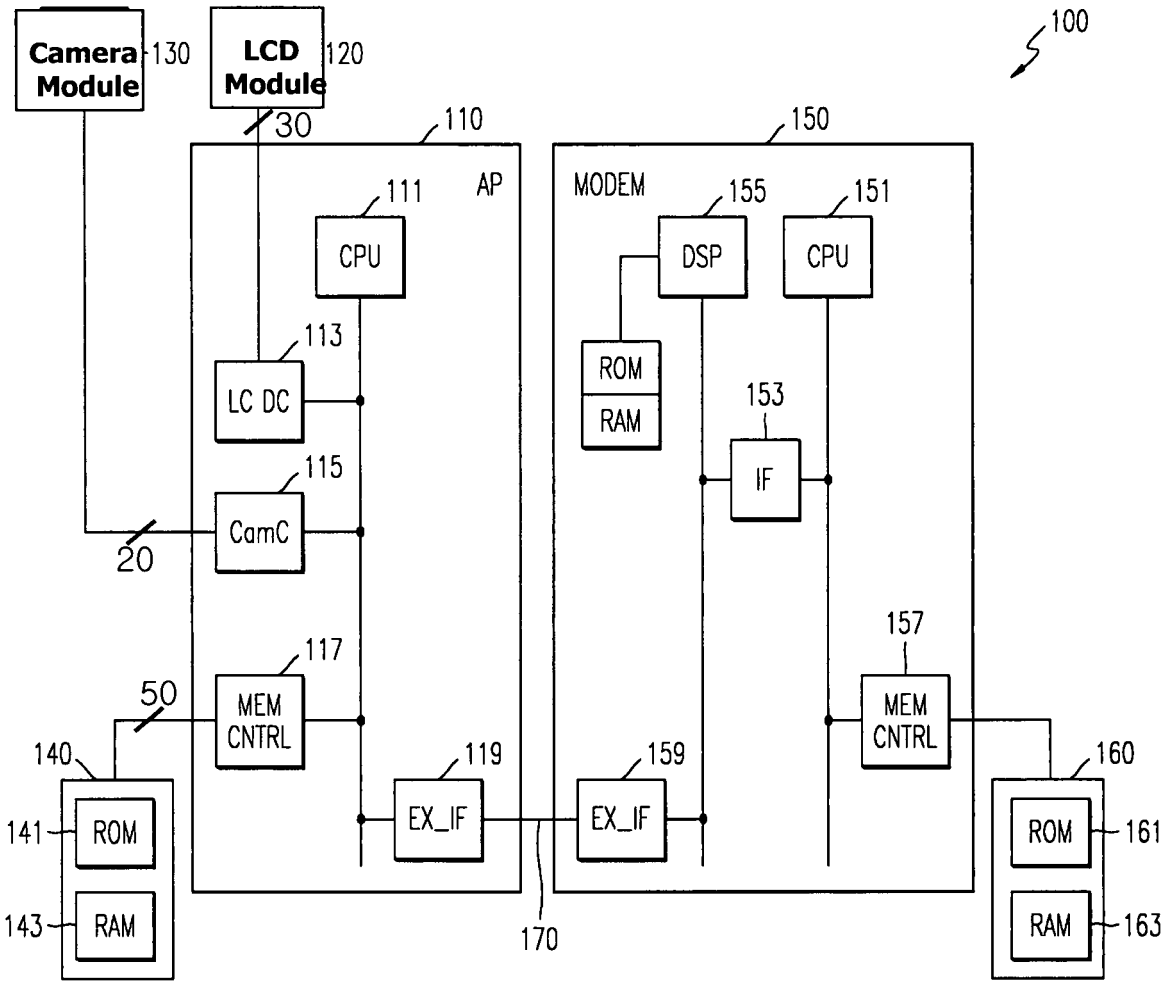
Camera Module
130
LCD Module
120
100
30
110
150
AP
111
CPU
MODEM
155
DSP
151
CPU
113
LC DC
ROM
RAM
153
IF
115
CamC
20
157
117
MEM CNTRL
50
140
119
159
160
MEM CNTRL
141
ROM
EX_IF
EX_IF
ROM
161
143
RAM
170
RAM
163

Fig. 2

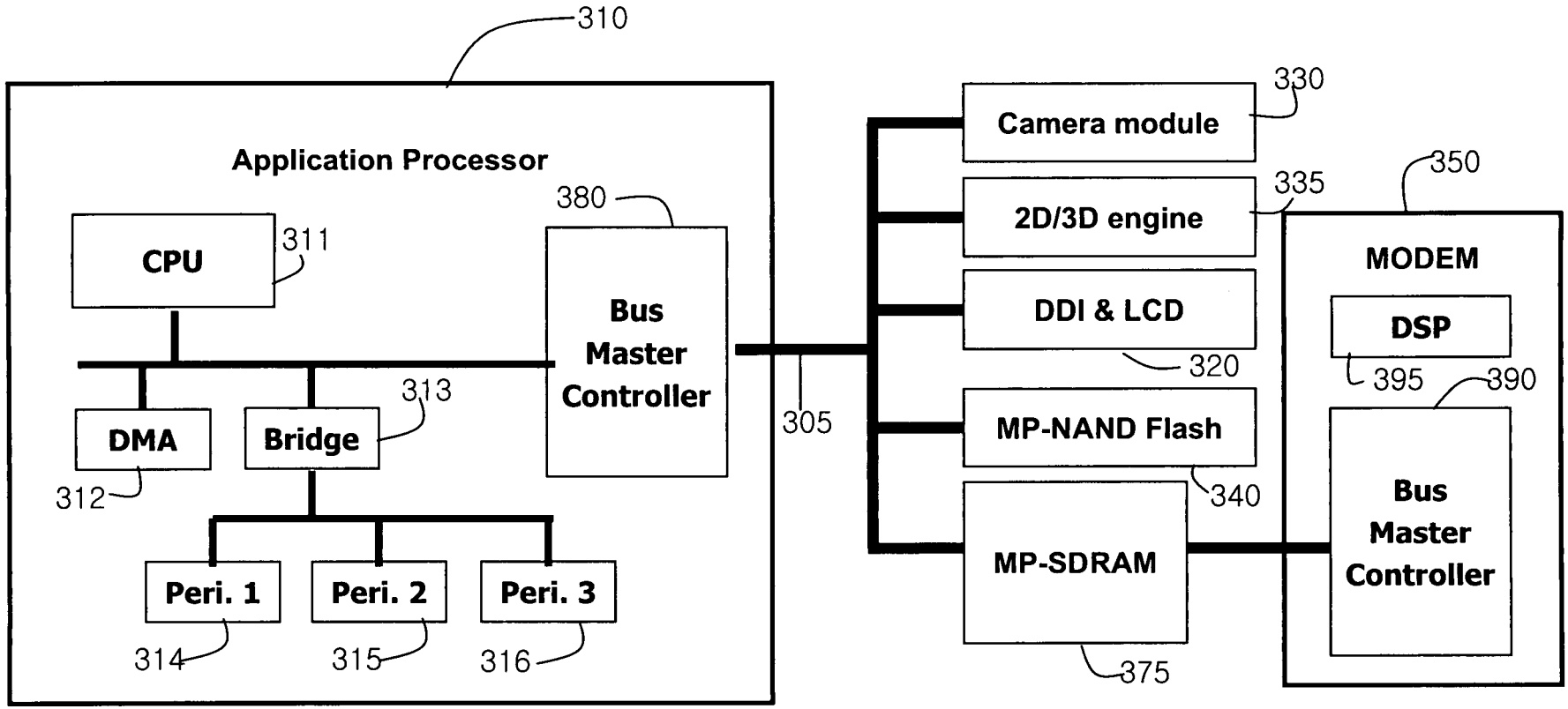
310
Application Processor
380
CPU
311
Bus
Master
Controller
DMA
312
Bridge
313
Peri. 1
314
Peri. 2
315
Peri. 3
316
305
Camera module
330
2D/3D engine
335
DDI & LCD
320
MP-NAND Flash
340
MP-SDRAM
375
350
MODEM
DSP
395
390
Bus
Master
Controller

Fig. 3

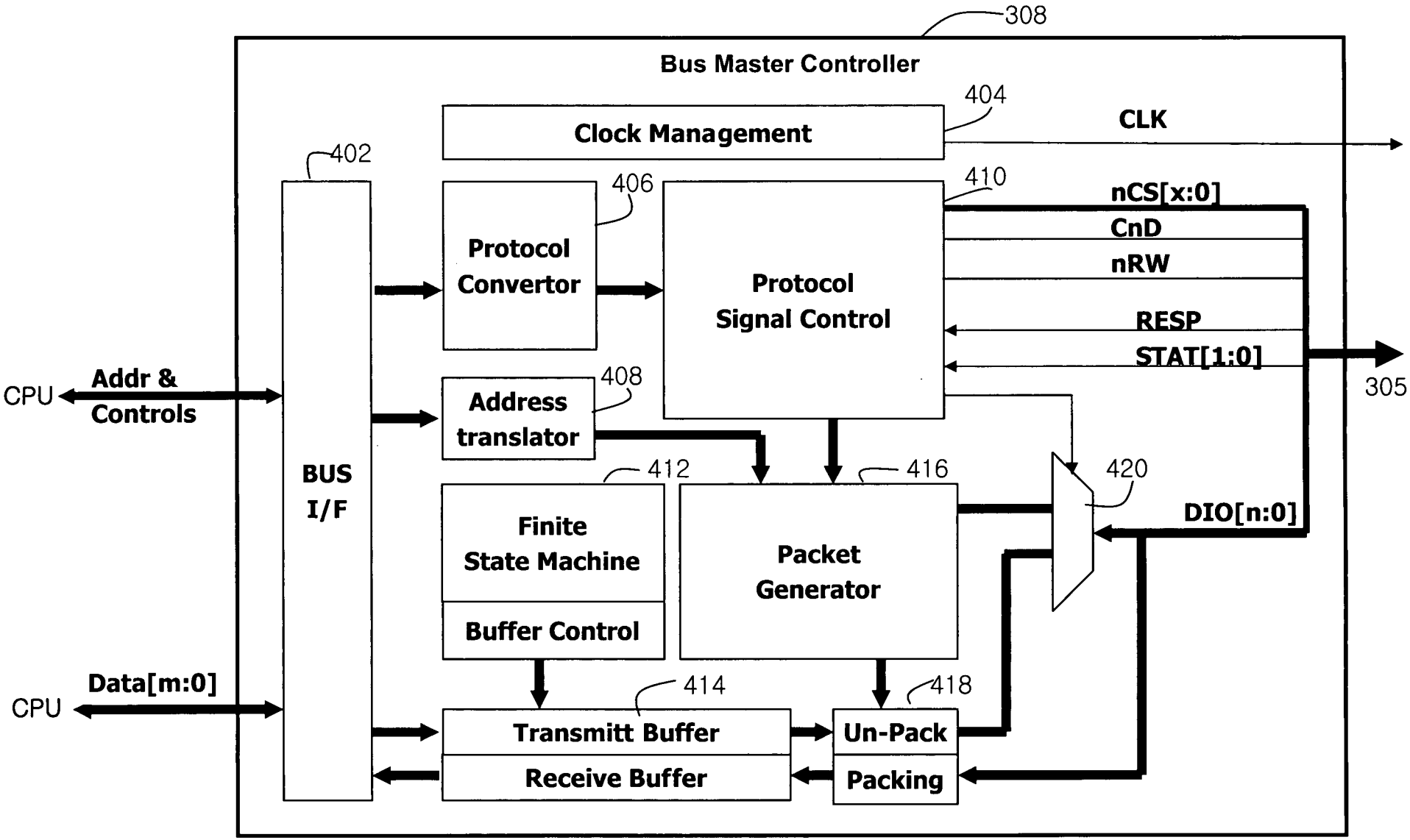
308
Bus Master Controller
404
Clock Management
CLK
402
406
410
Protocol Convertor
Protocol Signal Control
nCS[x:0]
CnD
nRW
RESP
STAT[1:0]
305
CPU
Addr & Controls
408
Address translator
BUS I/F
412
416
420
Finite State Machine
Packet Generator
DIO[n:0]
Buffer Control
CPU
Data[m:0]
414
418
Transmitt Buffer
Un-Pack
Receive Buffer
Packing

Fig.4

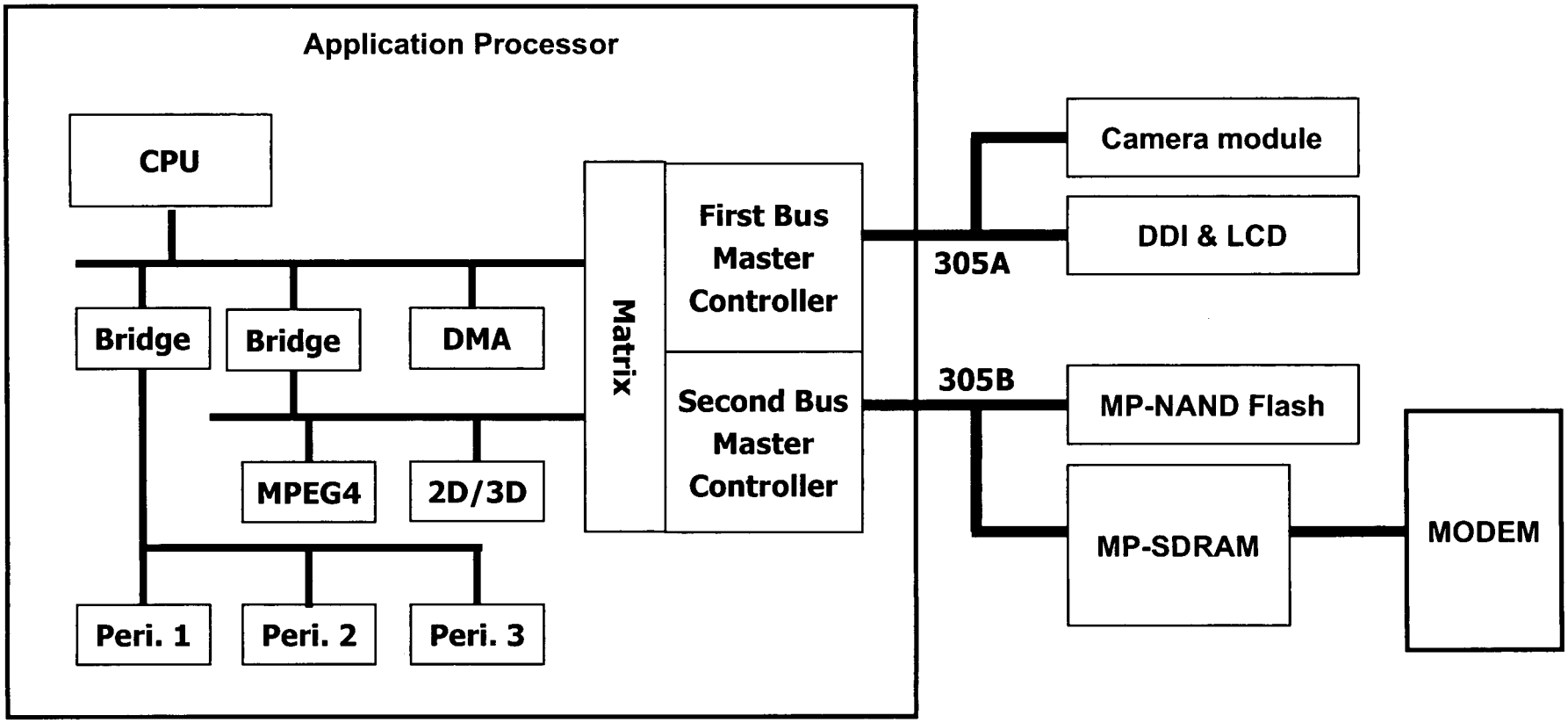
Application Processor
CPU
Bridge
Bridge
DMA
MPEG4
2D/3D
Peri. 1
Peri. 2
Peri. 3
Matrix
First Bus Master Controller
Second Bus Master Controller
305A
305B
Camera module
DDI & LCD
MP-NAND Flash
MP-SDRAM
MODEM

Fig.5

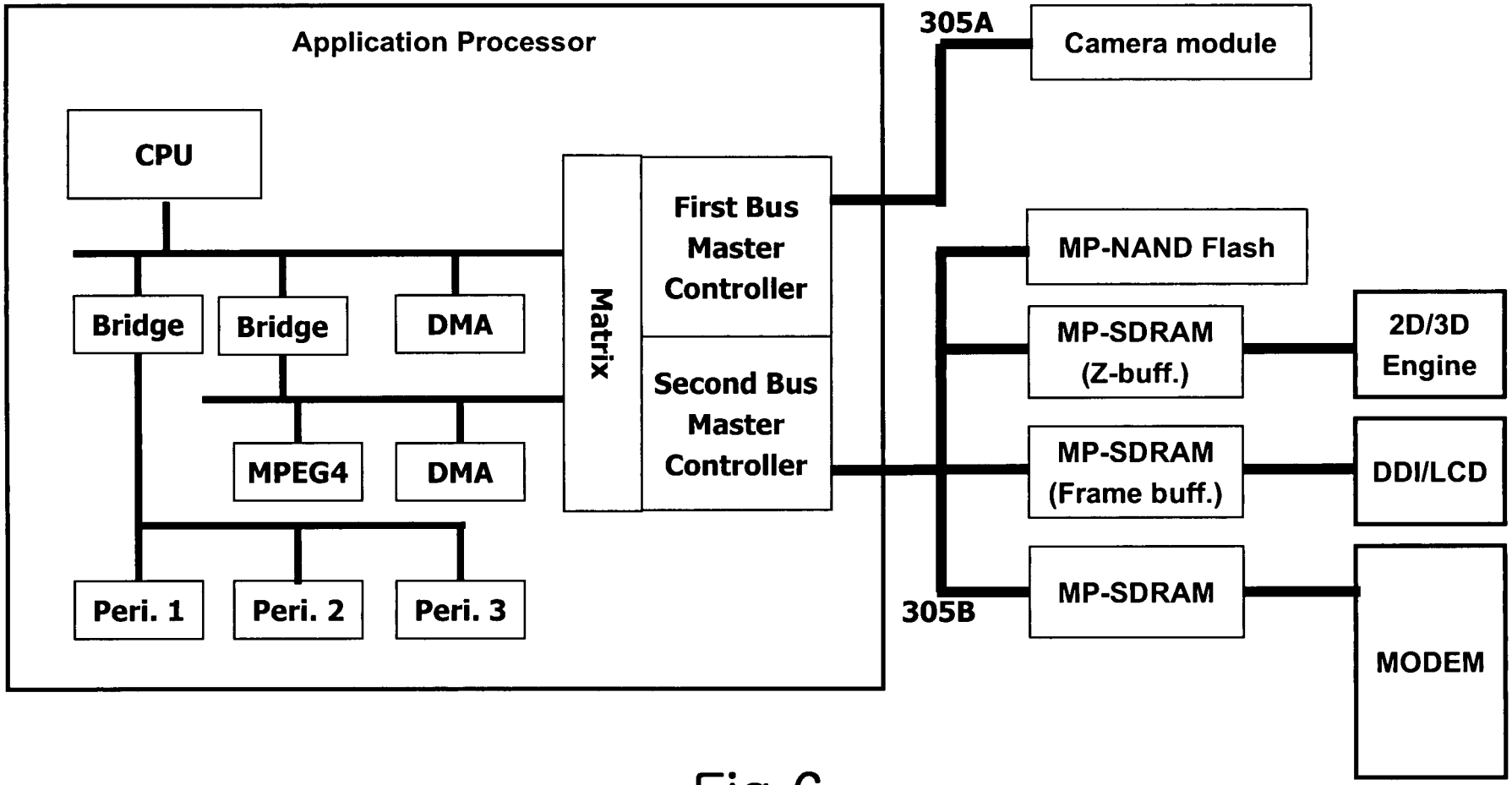
Application Processor
CPU
Bridge
Bridge
DMA
MPEG4
DMA
Peri. 1
Peri. 2
Peri. 3
Matrix
First Bus Master Controller
Second Bus Master Controller
305A
305B
Camera module
MP-NAND Flash
MP-SDRAM (Z-buff.)
MP-SDRAM (Frame buff.)
MP-SDRAM
2D/3D Engine
DDI/LCD
MODEM

Fig.6

Name	Signal Description
nCS	Chip Select signal, active low
CnD	Command Packet (High) or Data Packet (Low)
nRW	Transfer direction of the Data Pins (DIO) Master Write (High) or Read (Low)
CLK	Forwarded Clock, CMD & write-data packets are synchronized on this clock
DIO[3:0]	4-bit bi-directional data bus
RESP	Returned Clock, read-data packets are synchronized on this clock
STAT	Response of the Slave device

Fig.7

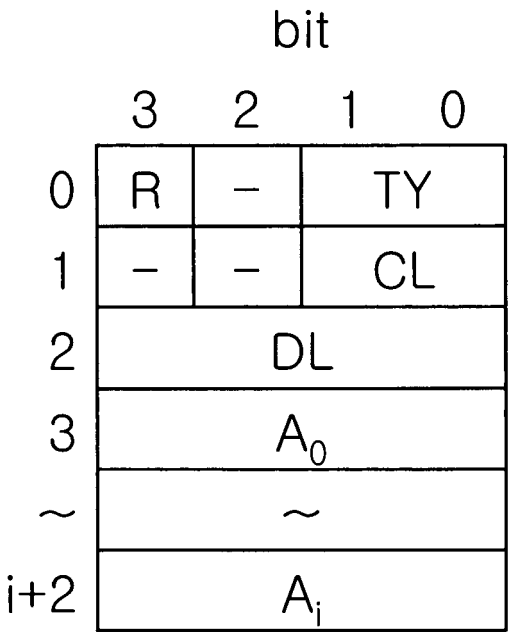

Fig.8

Field Name	Width	Description
R	1	This field specifies the target of the current transaction. The master can access the internal registers of the slave device or the actual data which will be supplied by the slave device. 0 – Access normal data 1 – Access the internal register of the slave device
TY	2	This field specifies the type of the current transfer. 00 – Read Transfer 01 – Reserved 10 – Write Transfer 11 – Reserved
CL	2	This field specifies the length of the CMD Packet. 00 – 4 x 4-bit 01 – 8 x 4-bit 10 – 12 x 4-bit 11 – 16 x 4-bit
DL	4	This field specifies the size of the Data Packet. Data-Packet Size = 2^DL bytes (1, 2 ~ 32,768 bytes)
$A_0 \sim A_i$	4 x (i+1)	These fields include the start address of the requested transfer

Fig.9

Address (byte)	Description
0	Manufacturer ID
1	
2	Version Number
3	Device Type
4	Max. Operational Frequency
5	
6	Master Command
7	Internal Buffer Control
8	Read Buffer Pending-Transaction Count
9	Write Buffer Pending-Transaction Count
A	Internal Buffer Size
B	
C	Write Buffer Base Address
D	
E	Reserved
F	Transaction Error

Fig.10

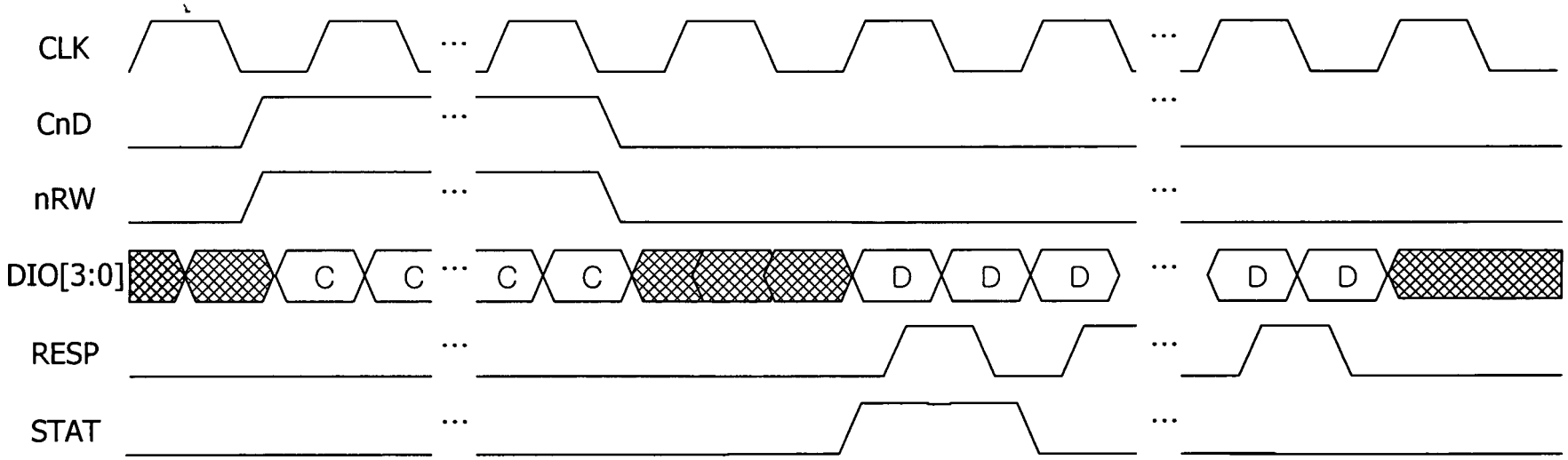

Fig.11

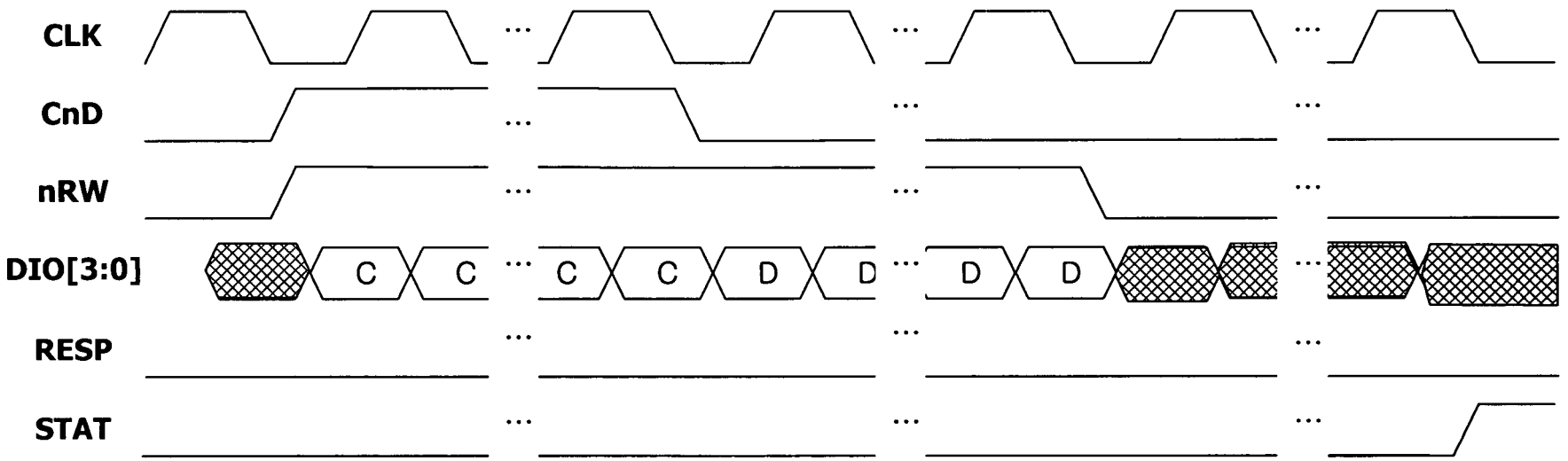

Fig.12

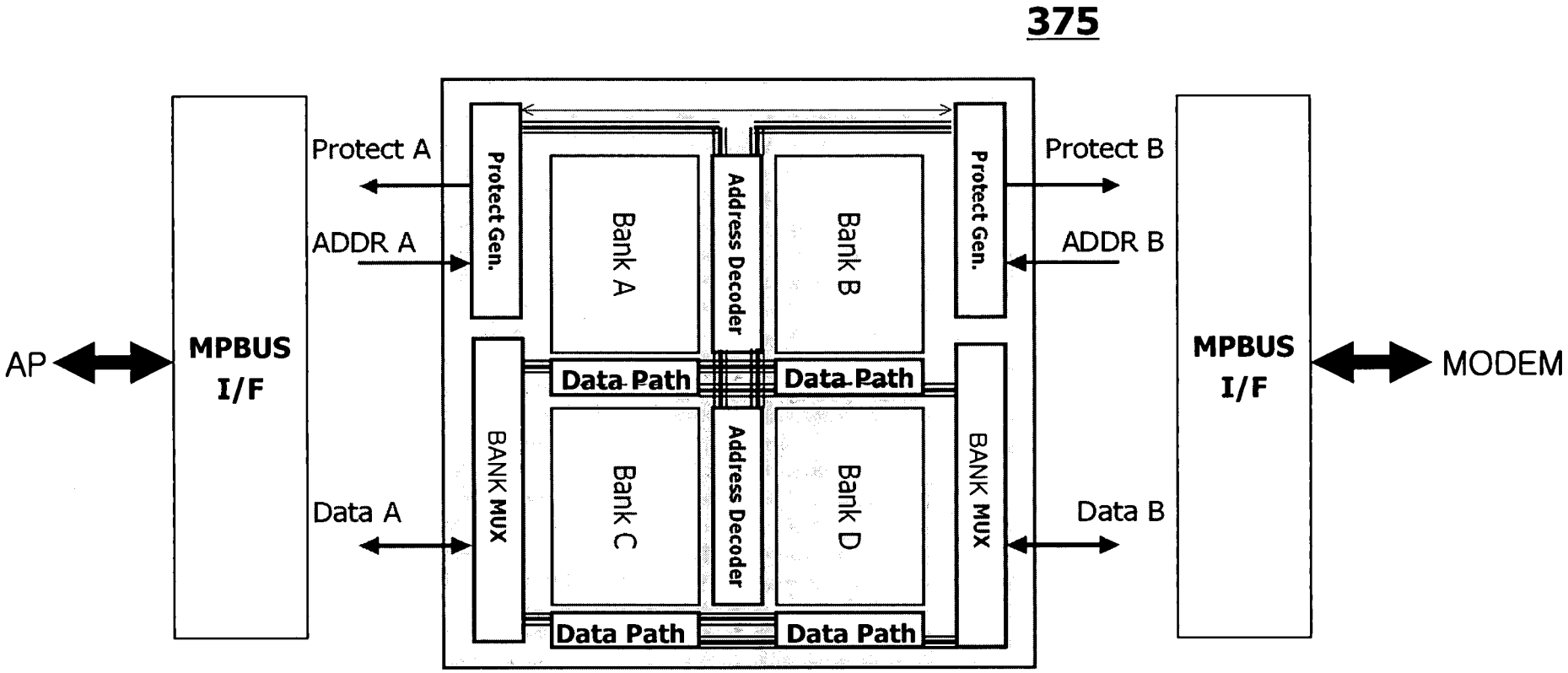
375
AP
MPBUS I/F
Protect A
ADDR A
Data A
Protect Gen.
BANK MUX
Bank A
Bank C
Address Decoder
Bank B
Bank D
Data Path
Data Path
Data Path
Data Path
Protect Gen.
BANK MUX
Protect B
ADDR B
Data B
MPBUS I/F
MODEM

Fig.13

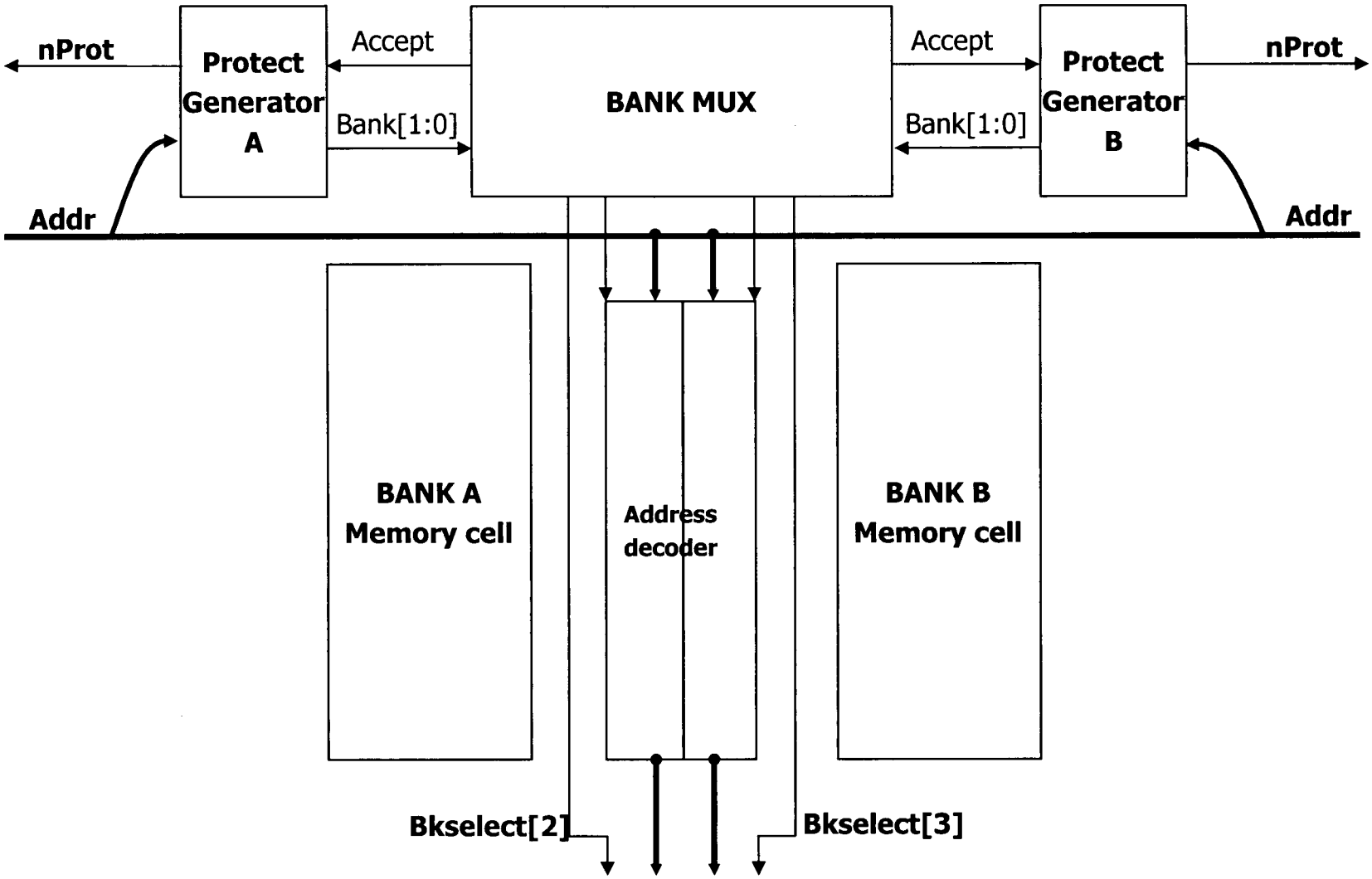
nProt
Protect Generator A
Accept
Bank[1:0]
BANK MUX
Accept
Bank[1:0]
Protect Generator B
nProt
Addr
Addr
BANK A Memory cell
Address decoder
BANK B Memory cell
Bkselect[2]
Bkselect[3]

Fig.14

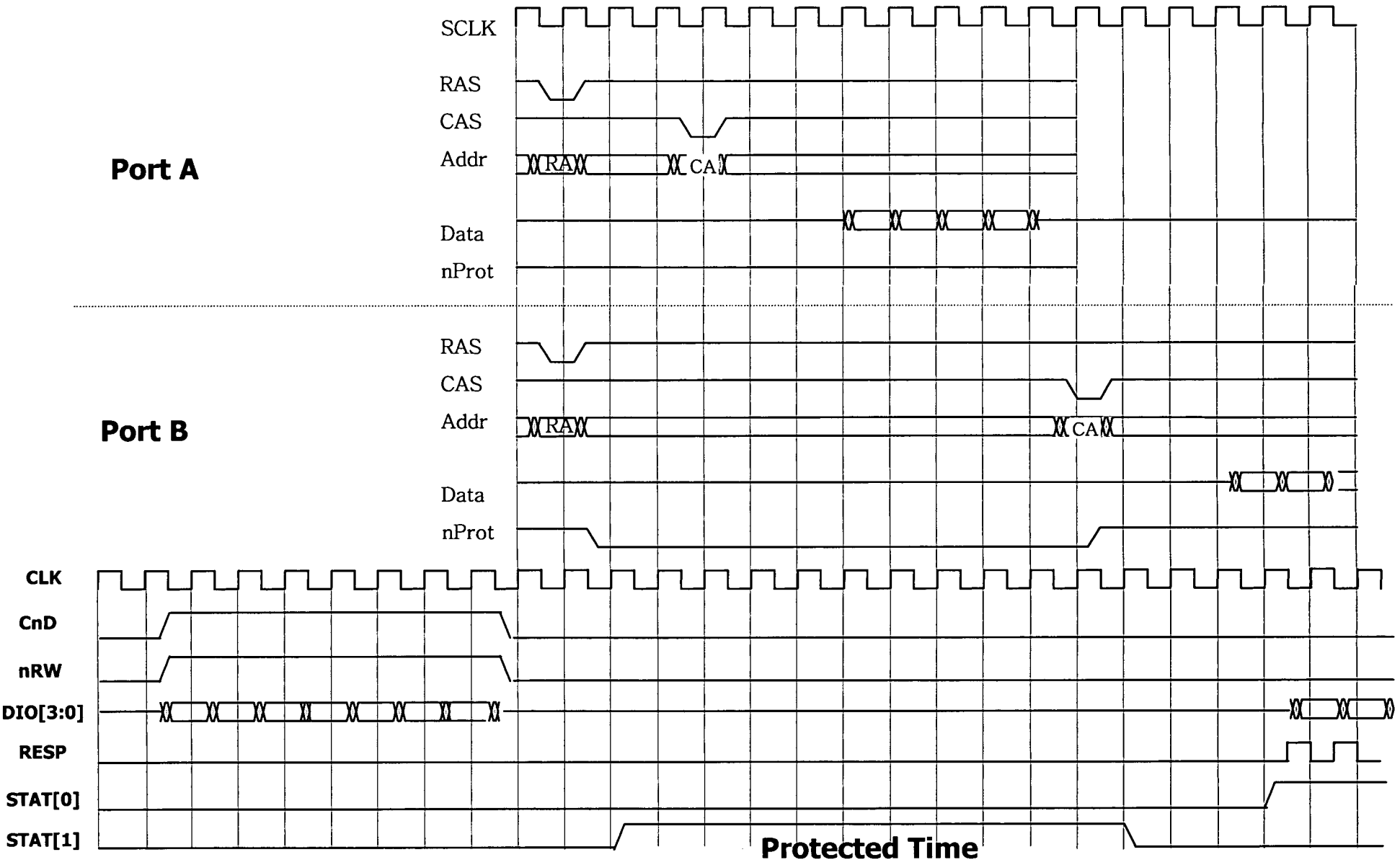
SCLK
RAS
CAS
Addr
RA
CA
Port A
Data
nProt
RAS
CAS
Addr
RA
CA
Port B
Data
nProt
CLK
CnD
nRW
DIO[3:0]
RESP
STAT[0]
STAT[1]
Protected Time

Fig.15